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Applicant: Jeremy A. Theil et al.
Title: Reducing Image Sensor Lag

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FIG. 1
(PRIOR ART)
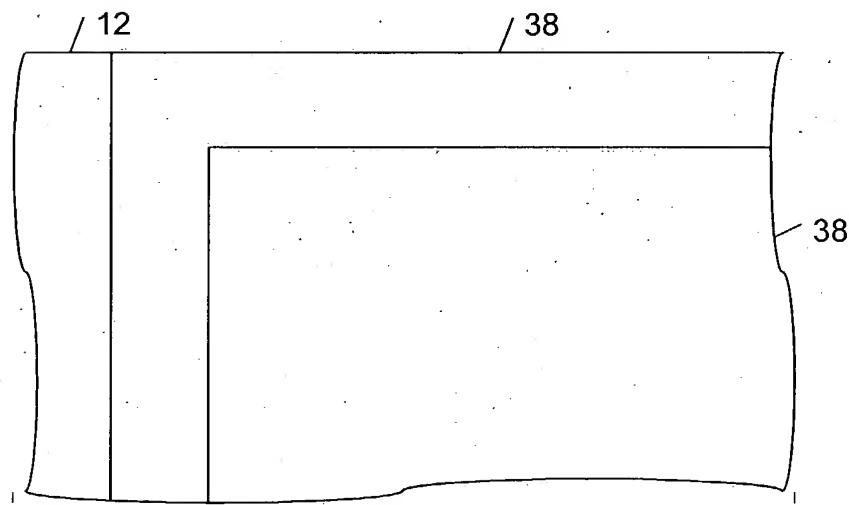
FIG. 2
(PRIOR ART)
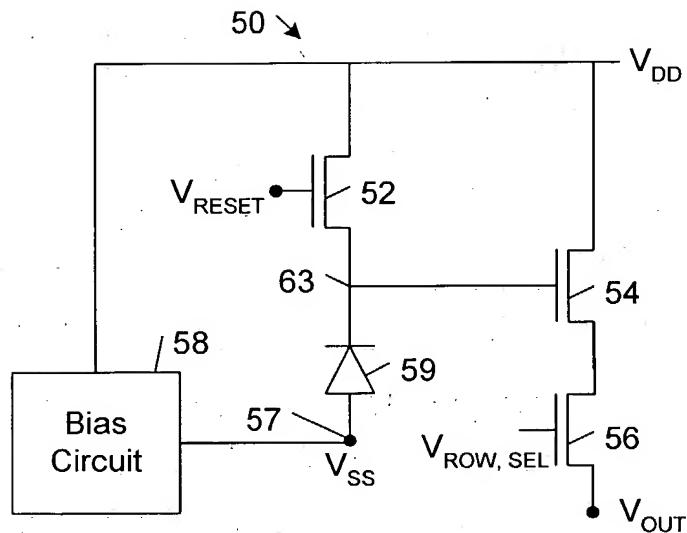
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50

V_{DD}

V_{RESET} — 52

63

54

58

59

Bias Circuit

57

V_{SS}

$V_{ROW, SEL}$ 56

V_{OUT}

FIG. 3
(PRIOR ART)

60 — Reset

61 — Readout

62 — Integrate

64 — Readout

FIG. 4
(PRIOR ART)

$V_{SS} < V_{DD}$

38

36

e^- e^- e^- e^-

h^+ h^+ h^+ h^+ h^+ h^+

34

38

I_R

20   32   18   30   16   28

16

21   21   21

14

V_{DD}

FIG. 5
(PRIOR ART)

FIG. 6

FIG. 7

FIG. 8

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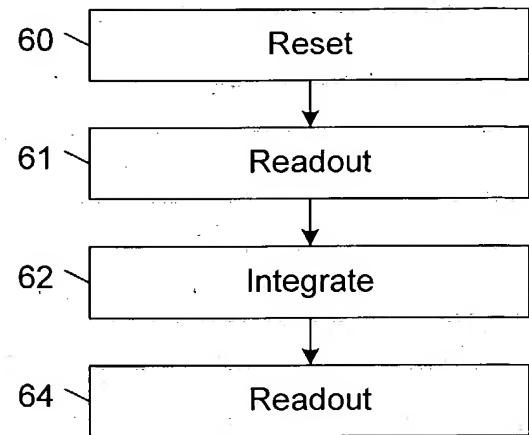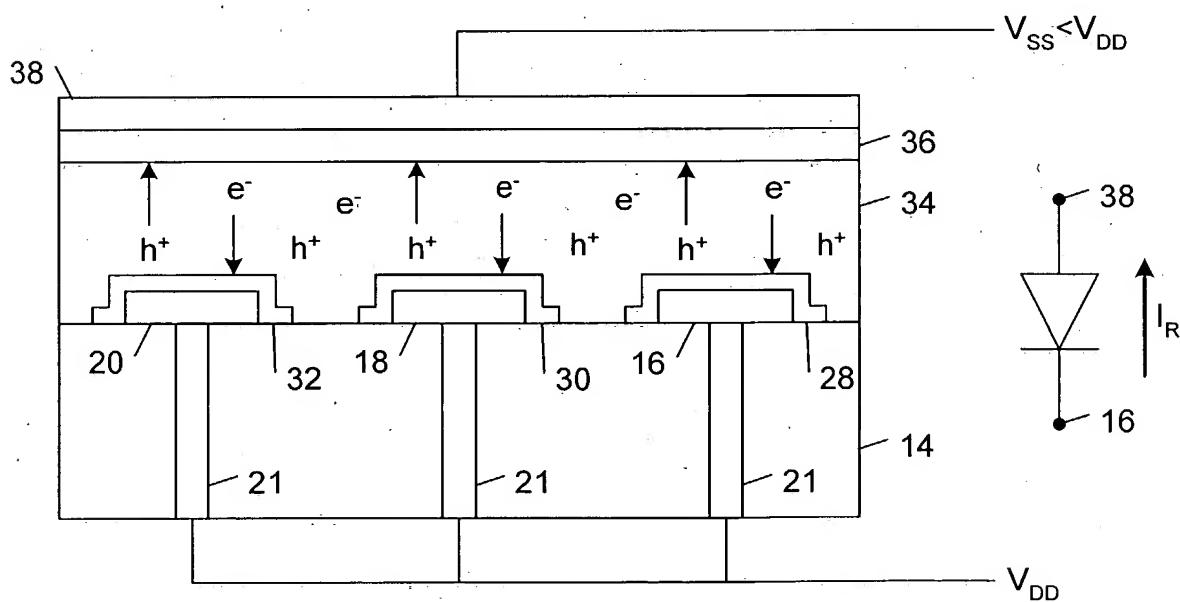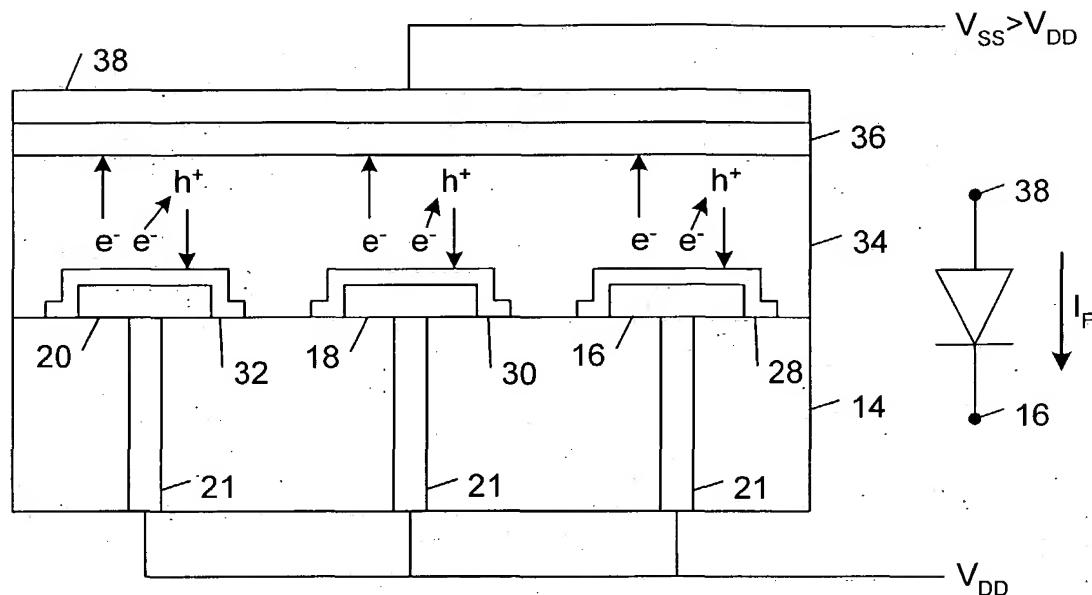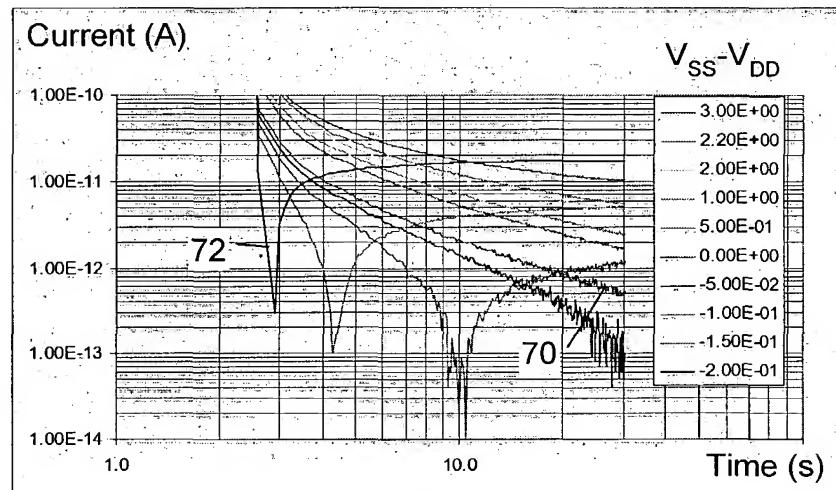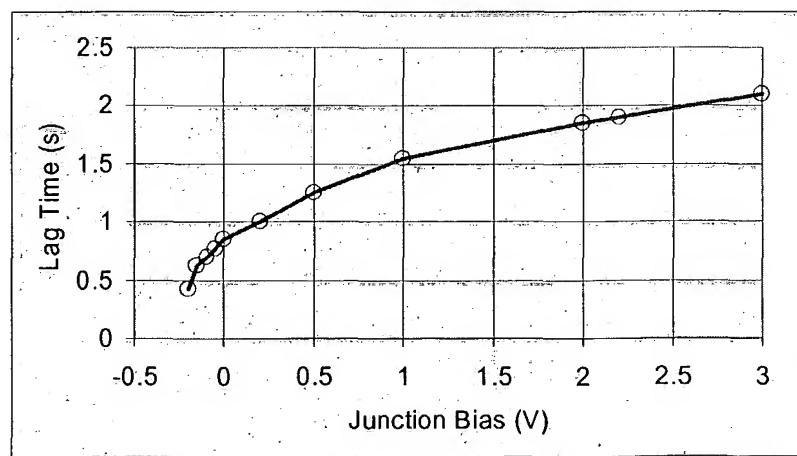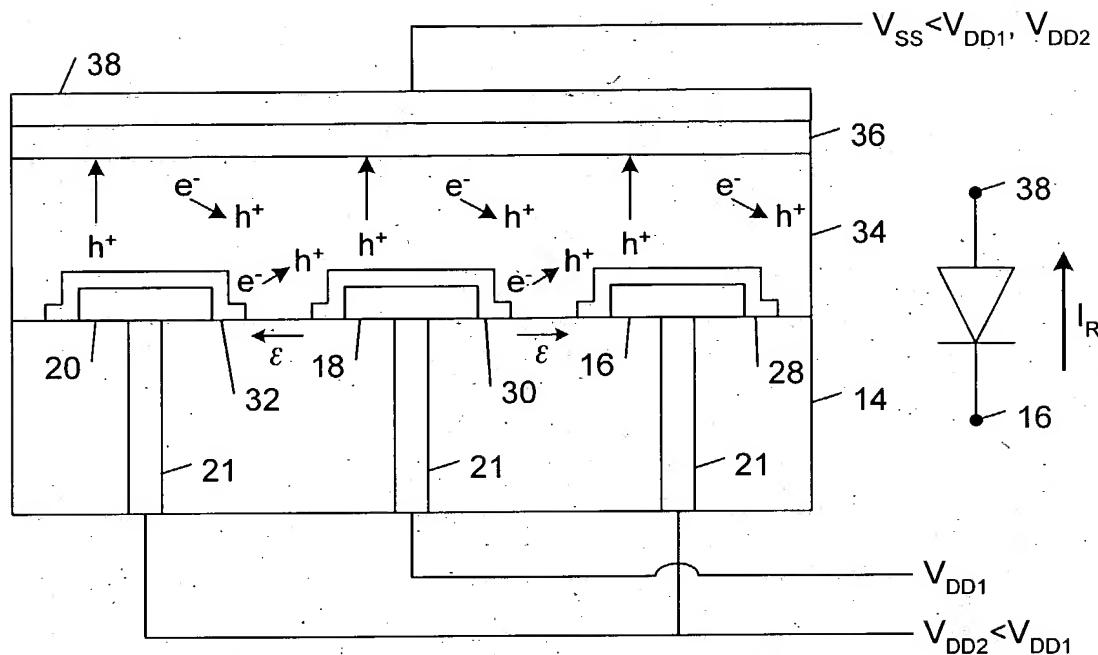
FIG. 9A
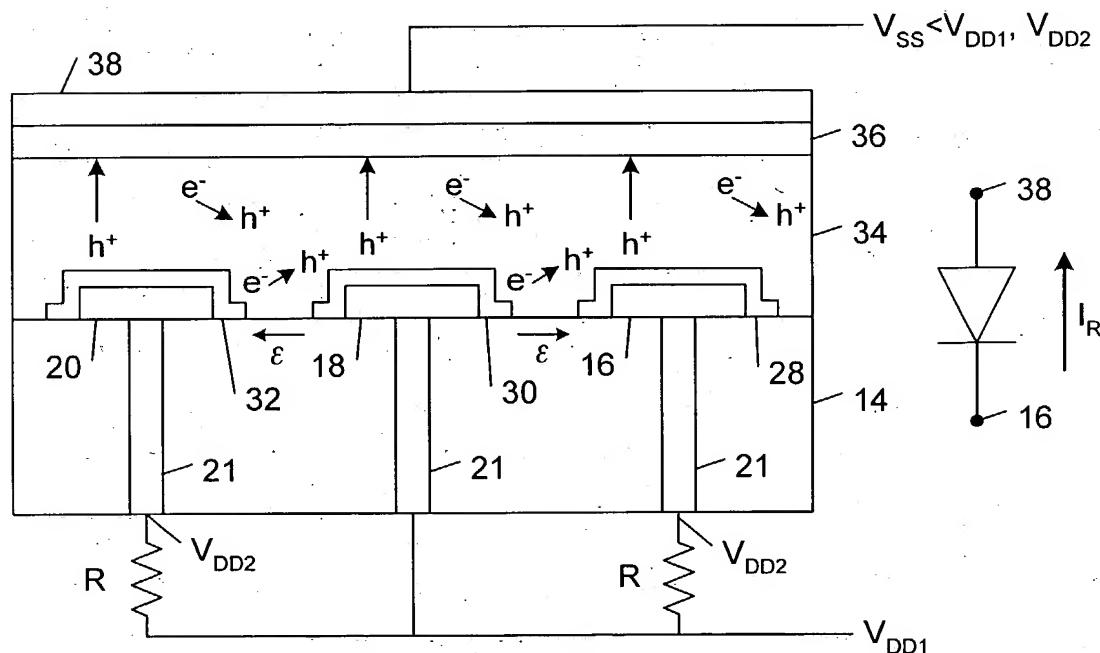
FIG. 9B
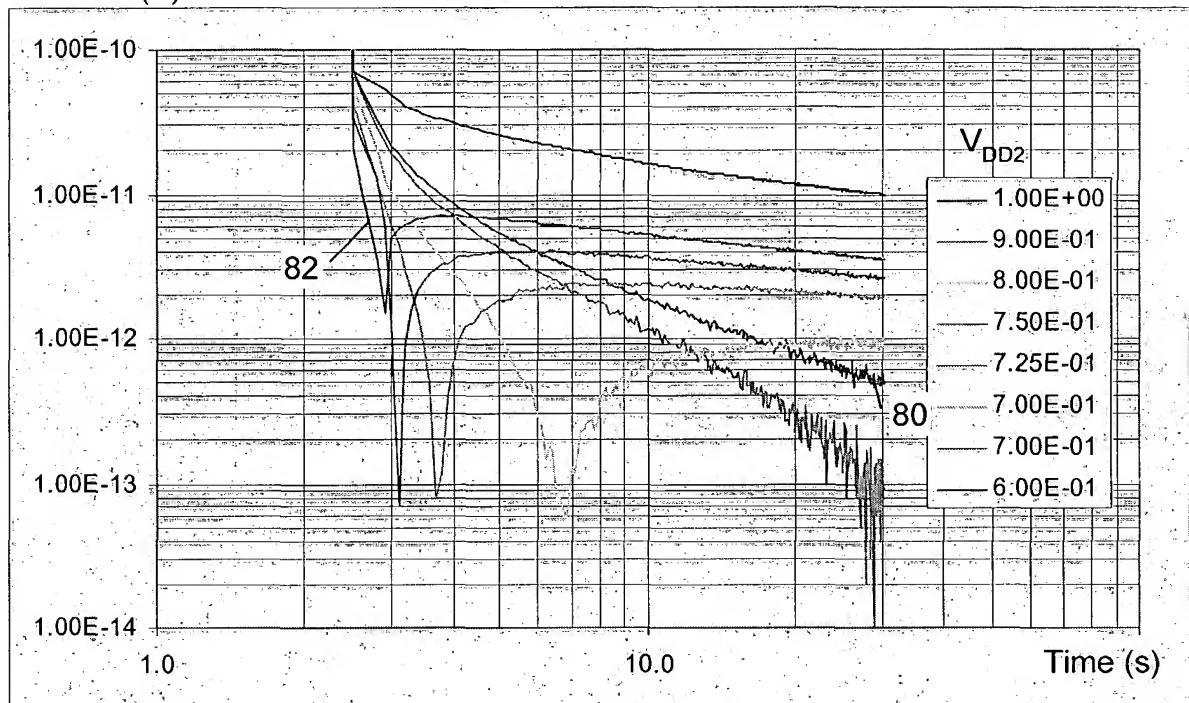
FIG. 10
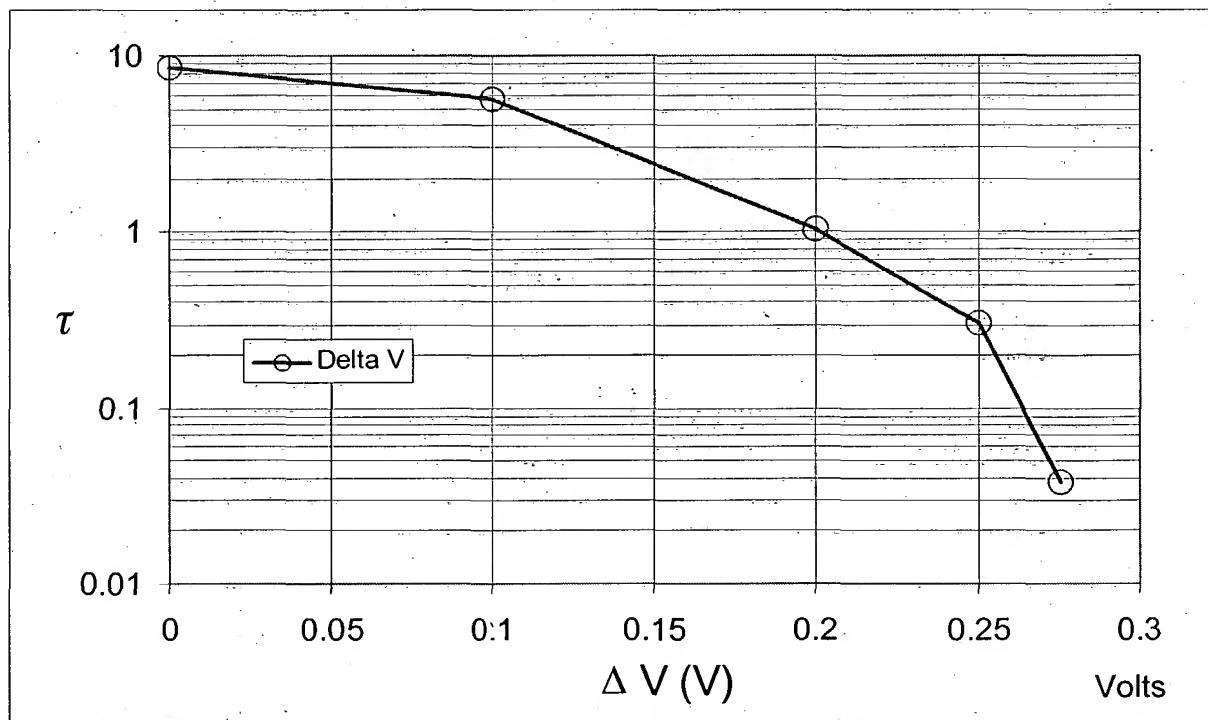
FIG. 11

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+	-	+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-	+	-

⋮

-	+	-	+	-	+	-	+	-	+

FIG. 12A

+	+	+	+	+	+	+	+	+	+
-	-	-	-	-	-	-	-	-	-
+	+	+	+	+	+	+	+	+	+

⋮

-	-	-	-	-	-	-	-	-	-

FIG. 12B